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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,604	10/31/2003	Noah Lassar	100202931-1	9859

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,604	LASSAR ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *20-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group I, claims 1-19, in the reply filed on 26 April 2006 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 10-14, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,777,855 (Yokajty).

Yokajty discloses, referring primarily to figures 2, 4, and 5, a connection assembly, comprising: a substrate assembly (30) and connection pads (46, 56) disposed on the substrate assembly to form a configuration capable of aligning each of the connection pads with a different terminal of a warped interconnect (60) [claim 1], wherein one or more of the connection pads are extended to each align with a different terminal of the warped interconnect (figures 4, 5) [claim 2], wherein one or more of the connection pads are extended to each align with a different terminal of the warped interconnect that is warped at a first end of the interconnect (figures 4, 5) [claim 3], wherein one or more of the connection pads are extended to each align with a different terminal of the warped interconnect that is warped at both a first end and a second end of the interconnect (figures 4, 5) [claim 4], wherein one or more of the connection pads

has a center that is offset from a line in a direction parallel to a surface of the substrate assembly upon which the connections pads are disposed, the line being defined by a plane perpendicular to the surface of the substrate assembly (best characterized by reference 34) [claim 5], wherein the configuration of the connection pads aligns each connection pad with a different terminal of a warped end of the interconnect (figures 4, 5) [claim 6], wherein the connection pads are solder pads (col. 3, lines 20-25 and col. 4, lines 10-15) [claim 7], wherein: the substrate assembly has at least a first surface upon which the connection pads are disposed; and the warped interconnect is warped in a direction parallel with the first surface of the substrate assembly (figures 4, 5) [claim 10], wherein: the substrate assembly has at least a first surface upon which the connection pads are disposed; and a first end of the warped interconnect is warped in a direction parallel with the first surface of the substrate assembly (figures 4, 5) [claim 11], wherein: the substrate assembly has at least a first surface upon which the connection pads are disposed; and a first end and a second end of the warped interconnect are both warped in a direction parallel with the first surface of the substrate assembly (figures 4, 5) [claim 12].

Similarly, Yokajty discloses, a connection assembly, comprising: a substrate assembly (30); and connection pads (46, 56) disposed on the substrate assembly to form a configuration that aligns each of the connection pads with a different terminal of an interconnect (60) such that a center of one or more of the connection pads is offset from a line in a direction parallel to a surface of the substrate assembly upon which the connection pads are disposed, the line being defined by a plane perpendicular to the

surface of the substrate assembly (best characterized by reference 34) [claim 13], wherein each of the connection pads align with a different terminal of the interconnect that is at least one of warped at a first end of the interconnect and warped at both the first end and a second end of the interconnect (figures 4, 5) [claim 14], wherein: the substrate assembly has a first surface upon which the connection pads are disposed; and the interconnect has non-linearly positioned terminals (since the flexible cable is curved, figures 2, 4, and 5, the terminals (46, 56) are non-linearly positioned) [claim 17].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8, 15, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokajty in view of US 2001/0033017 A1 (Wang).

Yokajty discloses the claimed invention as described above except Yokajty does not specifically disclose that the substrate assembly is a multilayered ceramic substrate assembly [claim 8]. However, it is well known in the art to form a printed circuit board substrate of multilayered ceramic as evidenced by Wang ([0019]). Therefore, it would have been obvious to one having ordinary skill in the art to form the substrate in the invention of Yokajty of multilayered ceramic as is known in the art and evidenced by Wang. The motivation for doing so would have been to use a multilayered structure for greater signal wiring density formed of ceramic for improved heat dissipation.

Similarly, regarding claim 15, Yokajty discloses the claimed invention as described above except Yokajty does not specifically disclose that the substrate assembly is a multilayered ceramic substrate assembly with conductive vias, and wherein the connection pads are solder pads each configured to form a soldered connection that electrically couples a terminal of the interconnect with a conductive via in the substrate assembly [claim 15]. However, it is well known in the art to form a printed circuit board substrate of multilayered ceramic having vias as evidenced by Wang (figure 2, [0019]). Therefore, it would have been obvious to one having ordinary

skill in the art to form the substrate in the invention of Yokajty of multilayered ceramic as is known in the art and evidenced by Wang. The motivation for doing so would have been to use a multilayered structure for greater signal wiring density formed of ceramic for improved heat dissipation. Additionally, it would have been obvious to one having ordinary skill in the art to connect the solder pads of Yokajty to the conductive vias as taught by Wang (figure 2). The motivation for doing so would have been to allow for signal transmission between the conductive layers and the flexible circuit.

Regarding claim 18, Yokajty discloses, a substrate assembly, comprising: a first surface; and connection pads (46, 56) disposed on the first surface to form a configuration such that each connection pad is configured to align with a different terminal (66) of an interconnect (60) that is warped in a direction parallel with the first surface. Yokajty does not specifically disclose conductive vias configured to electrically couple electronic components and the connection pads each configured to couple a different terminal of the interconnect with a conductive via [claim 18]. However, it is well known in the art to form a printed circuit board substrate of multilayered ceramic having vias as evidenced by Wang (figure 2, [0019]). Therefore, it would have been obvious to one having ordinary skill in the art to form the substrate in the invention of Yokajty of a multilayered structure as is known in the art and evidenced by Wang. The motivation for doing so would have been to use a multilayered structure for greater signal wiring density. Additionally, it would have been obvious to one having ordinary skill in the art to connect the solder pads of Yokajty to the conductive vias as taught by Wang (figure 2). The motivation for doing so would have been to allow for signal transmission

between the conductive layers and the flexible circuit. Additionally, the modified invention of Yokajty teaches that the connection pads are solder pads (Yokajty col. 3, lines 55-68) each configured to form a soldered connection that electrically couples a terminal of the interconnect with a conductive via [claim 19].

Claims 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokajty in view of US 5,375,041 (McMahon).

Yokajty discloses the claimed invention as described above except Yokajty does not specifically state that the warped interconnect is configured to interface at least one of an integrated circuit and an electronic component with the substrate assembly [claim 9]. However, it is well known in the art to use a flexible circuit to connect an electronic component to a circuit board as evidenced by McMahon (col. 2, lines 40-55). Therefore, it would have been obvious to one having ordinary skill in the art to use the flexible circuit of the invention of Yokajty to connect an IC to the circuit board as is known in the art and evidenced by McMahon. The motivation for doing so would have been to allow for the processing of signals from the circuit board by the IC.

Similarly, Yokajty discloses the claimed invention as described above except Yokajty does not specifically state that the interconnect is configured to interface at least one of an integrated circuit and an electronic component with the substrate assembly [claim 16]. However, it is well known in the art to use a flexible circuit to connect an electronic component to a circuit board as evidenced by McMahon (col. 2, lines 40-55). Therefore, it would have been obvious to one having ordinary skill in the art to use the

flexible circuit of the invention of Yokajty to connect an IC to the circuit board as is known in the art and evidenced by McMahon. The motivation for doing so would have been to allow for the processing of signals from the circuit board by the IC.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose warped interconnects:

US 6,452,112 B1 Terashima et al.,

US 6,472,607 B1 Someya et al.,

US 6,558,199 B2 Oguchi,

US 6,974,330 B2 Caldwell et al..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremy C. Norris
Patent Examiner

JCSN